REMARKS

Applicant submitted an Amendment and Response after Final Action on December 2, 2005, in response to the Final Office Action mailed on September 19, 2005. An Advisory Action was mailed on December 12, 2005, indicating that the proposed amendments would not be entered. Applicant respectfully requests that the December 2, 2005, Amendment and Response after Final Action not be entered with the accompanying Request for Continued Examination.

Status of the Claims

Claims 1 and 7-10 are pending. Claim 1 is currently amended to more clearly define pre-existing claim limitations. No claims are canceled. No claims are added. No new matter has been added.

Summary of the Office Action

Claim 1 stands objected to informalities.

Claims 1, 7, 8, and 10 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,204,524 to Rhodes (hereinafter "Rhodes")

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes '524 as applied to claims 1, 7, 8, and 10 above in view of U.S. Patent No. 5,973,375 to Baukus et al. (hereinafter "Baukus").

Response to Objections

Claim 1 stands objected to because of informalities. In particular, the Office Action states that claim 1 includes a typographical error. Applicant respectfully submits that claim 1 has been amended to address the objection. Applicant appreciates the Examiner's recommendation and respectfully requests that the objection to claim 1 be withdrawn.

Response to Rejections under 35 U.S.C. § 102(e)

The Office Action rejected claims 1, 7, 8, and 10 under 35 U.S.C. § 102(e) as being anticipated by Rhodes. Applicant respectfully requests withdrawal of these rejections because the cited reference fails to disclose all of the limitations of the claims.

CLAIMS 1, 7, 8, AND 10

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Rhodes. Applicant respectfully submits that claim 1 is patentable over the cited reference because Rhodes does not disclose all of the limitations of the claim. Claim 1, as amended, recites:

> A pixel structure comprising:
>
> a semiconductor substrate;
>
> a radiation sensitive source of carriers in the substrate;
>
> **a region in the substrate for collecting** but not storing the carriers;
>
> at least one doped or inverted region of a first conductivity in or on the substrate; and
>
> at least one planar current flow, carrier transport pathway from or through the region in the substrate for collecting but not storing carriers, to the at least one doped or inverted region, in which carrier transport pathway carriers are not stored, there being no means for storing carriers in between the region for collecting but not storing carriers and the at least one planar current flow, carrier transport pathway, **wherein substantially all of the region for collecting but not storing carriers is in the substrate under a polysilicon gate electrode**.

(Emphasis added).

In support of the rejection, the Office Action states, in part:

> . . . Rhodes discloses (see, for example, FIG 5) a pixel cell (pixel structure) 114 comprising a substrate, radiation sensitive source of carriers in the substrate, **transfer region (region in the substrate for collecting but not storing carriers) 126**, floating region of a second conductivity type (one doped or inverted region) 130, and the planar current flow, carrier transport pathway.
>
> Regarding the limitation "wherein the region for collecting but not storing carriers is substrate under a polysilicon gate electrode", see column 8, line 41-51 wherein Rhodes discloses the **conductive layer (polysilicon gate electrode) 108 comprising polysilicon and part of transfer gate stack 128**.

Office Action, September 19, 2005, pp. 2-3 (emphasis added).

Applicant respectfully disagrees with the Office Action's characterization of Rhodes. In particular, Rhodes does not disclose a region in the substrate for collecting

and wherein substantially all of the region for collecting but not storing carriers is under a polysilicon gate electrode.

Rhodes is directed to a CMOS imager with a charge capacitor to facilitate improved signal-to-noise ratio and dynamic range. (Rhodes, Abstract). The storage capacitor is formed in conjunction with a pixel cell. (Rhodes, col. 7, line 65 to col. 8, line 2). The pixel cell includes five doped regions. (Rhodes, col. 7, lines 30-33). The first doped region 110 is associated with the photogate 102 to form a photogate transistor 125. (Rhodes, col. 7, lines 33-36). The photogate is where photo-generated charge is accumulated. (Rhodes, col. 2, lines 1-5). The second doped region 126 electrically connects the photogate transistor 125 to the transfer transistor 128. (Rhodes, col. 7, lines 36-38). The second doped region 126 is also called a transfer region. (Rhodes, col. 9, lines 9-10). Rhodes fails to disclose any other functions of the transfer region 126 other than to electrically connect the photogate transistor 125 to the transfer transistor 128. In particular, Rhodes does not teach the transfer region 126 as capable of accumulating a photo-generated charge. Rather, the photogate transistor 125, which includes the first doped region 110, collects the photo-generated charge. The transfer region 126 merely transfers, but does not collect, an electrical charge. Therefore, the transfer region 126 of Rhodes is not a region in the substrate for collecting but not storing the carriers.

For the sake of argument, even if the transfer region 126 were to collect an electrical charge, Rhodes fails to disclose wherein substantially all of the region for collecting but not storing carriers is under a polysilicon gate electrode. Rhodes illustrates the process for fabricating the pixel cell and storage capacitor in Figures 6-14. (Rhodes, col. 7, lines 28-30). Rhodes teaches fabricating the storage capacitor and pixel cell in the following order:

1. Substrate 116 (Fig. 6)
2. Doped Substrate 120 (Fig. 6)
3. Doped Region 110 (Fig. 6)
4. Insulating Layer 100 (Fig. 7, the insulating layer 100 is misnumbered as the insulating layer 110)
5. **Conductive Layers 108** (Fig. 8)
6. Insulating Sidewalls 112 (Fig. 8)
7. **Doped Regions 126**, 130, 134, and 155 (Fig. 8)

The disclosed fabrication process provides in detail that the transfer region 126 is not doped until after the conductive layer 108. Furthermore, the transfer region 126 is offset relative to the conductive layer 108. At most, the transfer region 126 is shown under the insulating sidewall adjacent to the conductive layer 108. The approximate alignment in Figure 6 of the rightmost vertical line of the transfer region 126 with the rightmost vertical line of the insulating sidewall 112 adjacent to the conductive layer 108 does not teach the transfer region 126 under the conductive layer 108. In fact, the specification of Rhodes is silent as to any relationship between the transfer region 126 and the conductive layer 108. Nevertheless, it is understood from the detailed disclosure of the fabrication process that the transfer region 126 is offset from and doped after the conductive layer 108 is fabricated. Therefore, the transfer region 126 is not located under the conductive layer. Moreover, even if a slight overlap were to exist, Rhodes does not teach substantially all of the transfer region 126 under the conductive layer 108. Therefore, Rhodes fails to disclose wherein substantially all of the region for collecting but not storing carriers is under a polysilicon gate electrode.

In contrast, claim 1 recites "a region in the substrate for collecting" and "wherein substantially all of the region for collecting but not storing carriers is under a polysilicon gate electrode." For the reasons stated above, Rhodes fails to disclose all of the limitations of claim 1. In particular, Rhodes does not disclose a region in the substrate for collecting and wherein substantially all of the region for collecting but not storing carriers is under a polysilicon gate electrode. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 1 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 1 under 35 U.S.C. § 102(e) be withdrawn.

Given that claims 7-10 depend from independent claim 1, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 7-10 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 7, 8, and 10 under 35 U.S.C. § 102(e) and the rejection of claim 9 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Jeffrey Holman at (408) 720-8300.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

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Date: 12/16/05

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